FPGA IMPLEMENTATION OF IMAGE PROCESSING 2D CONVOLUTION FOR SPATIAL FILTER

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Specially dedicated to my family, lecturers, fellow friends and those who have guided and inspired me throughout my journey of education

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ABSTRACT

Computer manipulation of images is generally defined as digital image processing (DIP). DIP is used in variety of applications, including video surveillance, target recognition, and image enhancement. Some of the many algorithms used in image processing include convolution, edge detection and contrast enhancement. These are usually implemented in software but may use special purpose hardware for speed. With advances in the VLSI technology hardware implementation has become an attractive alternative. Assigning complex computation tasks to hardware and exploiting the parallelism and pipelining in algorithms yield significant speedup in running times. The main objective of this project is to develop an image processing algorithm, 2D convolution. The algorithm is designed and implemented in synthesizable Verilog HDL. Upon completion of the coding, its functionality and timing are then verified thoroughly. Subsequently, the performance of the 2D convolution is analyzed. The designed 2D convolution applies pipeline and parallel architecture for speedup and real-time applications. The entire design process starts with architecture definition and design. Once the required modules and functionalities such as DU and CU are defined, they are then coded and integrated. Verification is done from bottoms up starting from individual sub-modules. In addition, the design is further verified with real image pixels and compared the output pixels with that obtained from software (MATLAB). Altera Quartus II compilation report shows the 2D convolution design acheieves *fmax* as high as 394MHz using off-chip RAM. The performance is slighly degraded, to about 322MHz with on-chip RAM.

ABSTRAK

Komputer manipulasi imej secara amnya ditakrifkan sebagai pemprosesan imej digital (DIP). DIP digunakan dalam pelbagai aplikasi, termasuk pengawasan video, pengesahan sasaran, dan peningkatan kualiti imej. Banyak algoritma digunakan dalam pemprosesan imej termasuk convolution, pengesahan pinggir imej dan peningkatan kontras imej. Biasanya algoritma ini dilaksanakan dalam perisian (sofware), malah ia juga dilaksanakan dalam perkakasan (hardware) dengan tujuan untuk mencapai kelajuan dalam perlaksanaan algoritma. Dengan kemajuan dalam teknologi VLSI, perlaksanaan perkakasan telah menjadi satu alternatif yang amat menarik. Melaksanakan tugas-tugas pengiraan yang kompleks dalam perkakasan, dan mengeksploitasi parallelism dan pipeline dalam algoritma memberikan kecepatan ketara. Objektif utama projek ini adalah untuk membina satu algoritma pemprosesan imej, iaitu convolution dua-dimensi (2D). Algoritma tersebut telah direkabentuk dan dilaksanakan dalam bahasa Verilog HDL. Setelah proses rekaan selesai, fungsinya akan diuji dan prestasiny turut dianalisis. 2D convolution ini menggunakan pipeline dan seni-bina selari untuk mencapai kecepatan dan real-time aplikasi. Proses pembangunan bermula dengan definisi seni-bina dan reka-bentuk. Selepas itu, fungsi dan modul-modul utama seperti DU dan CU akan ditakrifkan dan direka-bentuk. Kemudian, merekan telah digabungkan untuk membina 2D convolution. Ujian terhadap rekaan akan dilakukan dari bawah, iaitu bermula dengan modul asas. Di samping itu, system tersebut juga diuji and disahkan fungsinya dengan menggunakan piksel imej, seterusnya membandingkan piksel output yang diperolehi dengan output daripada perisian (MATLAB). Laporan kompilasi daripada Altera Quartus II menunjukkan bahawa reka-bentuk 2D convolution ini mencapai *fmax* sebanyak 394MHz menggunakan off-chip RAM. Walaubagaimanapun, prestasinya akan turun kepada 322MHz dengan on-chip RAM.